REMARKS

The present Amendment amends claim 1, cancels claim 12, and leaves claims 8 and 9 unchanged. Therefore, the present application has pending claims 1, 8 and 9.

Title

The Examiner objected to the title of the invention, asserting that a new title is required that is clearly indicative of the invention to which the claims are directed. Applicants have amended the title to overcome this objection. Therefore, this objection should be withdrawn.

35 U.S.C. §112 Rejections

Claim 12 is rejected under 35 U.S.C. §112, first paragraph as allegedly failing to comply with the written description requirement. As indicated above, claim 12 was canceled. Therefore, the rejection regarding claim 12 is rendered moot.

35 U.S.C. §102 Rejections

Claims 1, 8 and 9 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,964,869 to Talcott et al. ("Talcott"). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1, 8 and 9 are not taught or suggested by Talcott whether taken individually or in combination any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, amendments were made to the claims to more

clearly recite that the present invention is directed to a data processing device, as recited, for example, in independent claim 1.

The present invention, as recited in claim 1, provides a data processing device that decodes and executes instructions of a predetermined length instruction set, which contain a spare field. The data processing device includes an instruction cache memory, a predecode-processor, and an instruction flow unit. The predecode-processor decodes operation codes contained in first fields of each of the instructions, so as to generate a piece of information. The information represents whether the instruction is a branch instruction or not. The predecode-processor also transfers the information as the spare field of each of the instructions. According to the present invention, the instruction cache memory holds the information in the spare field of each of the instructions. The instruction flow unit controls an executing sequence of the instructions based on information of the spare field, when executing instructions loaded from the cache memory. Also in the data processing device, the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that the instruction is a branch instruction, based on the information of the spare field. Furthermore, according to the present invention, the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set. The prior art does not disclose all these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record, particularly Talcott, whether taken individually or in combination with any of the other references of record.

Talcott teaches an instruction fetch mechanism having simultaneous prediction of control-flow instructios. However, there is no teaching or suggestion in Talcott of the data processing device as recited in claim 1 of the present invention.

In Talcott, a microprocessor is provided with an instruction fetch mechanism that simultaneously predicts multiple control-flow instructions. The instruction fetch unit further is capable of handling multiple types of control-flow instructions. The instruction fetch unit uses predecode data and branch prediction data to select the next instruction fetch bundle address. If a branch misprediction is detected, a corrected branch target address is selected as the next fetch bundle address. If no branch misprediction occurs and the current fetch bundle includes a taken control-flow instruction, then the next fetch bundle address is selected based on the type of control-flow instruction detected. If the first taken control-flow instruction is a return instruction, a return address from the return address stack is selected as the next fetch bundle address. If the first taken control-flow instruction is an unconditional branch or predicted taken conditional branch, a predicted branch target address is selected as the next fetch bundle address. If no branch misprediction is detected and the current fetch bundle does not include a taking control-flow instruction, then a sequential address is selected as the next fetch bundle address.

Features of the present invention, as recited in claim 1 include where the predecode-processor decodes operation codes contained in first fields of each of the instructions, so as to generate a piece of information. The information represents whether the instruction is a branch instruction or not. The predecode-processor also sets the information in the spare field of each of the instructions. According to the present invention, the instruction cache memory holds the information in the spare

field of each of the instructions. Talcott does not disclose these features. For example, Talcott does not teach or suggest where the instruction cache memory holds the information in the spare field of each of the instructions, in the manner claimed. In the present invention, the instruction cache memory holds the information in the spare field, where the information represents whether or not the instruction is a branch instruction or not, and where the spare field is a reserved field or an open field in the instructions of predetermined length instruction. This structure does not need to increase the capacity of the instruction cache because of the use of the spare field to temporarily store information of various types in that field. To the contrary, Talcott needs an extra memory device or memory area (see, e.g., the TBAT 208 and column 8, line 8-23). Therefore, Talcott does not disclose the use of a spare field in the instructions of predetermined length instruction set, as in the present invention.

Other features of the present invention, as recited in claim 1, include where the instruction flow unit controls an executing sequence of the instructions based on information of the spare field, when executing instructions loaded from the cache memory. Also in the data processing device, the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that the instruction is a branch instruction, based on the information of the spare field. Furthermore, according to the present invention, the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set. Talcott does not disclose these features. For example, Talcott does not teach or suggest where the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set, as in the present invention. As previously

discussed, the instruction cache memory of the present invention holds the information in the spare field, where the information represents whether or not the instruction is a branch instruction or not, and where the spare field is a reserved field or an open field in the instructions of predetermined length instruction. This structure does not need to increase the capacity of the instruction cache because of the use of the spare field to temporarily store information of various types in that field. To the contrary, Talcott needs an extra memory device or memory area (see, e.g., the TBAT 208 and column 8, lines 8-23). Therefore, Talcott does not disclose the use of a spare field in the instructions of predetermined length instruction set, as in the present invention.

Therefore, Talcott fails to teach or suggest "a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and sets the information in said spare field of each of said instructions" and "wherein the instruction cache memory holds the information in said spare field of each of said instructions" as recited in claim 1.

Furthermore, Talcott fails to teach or suggest "an instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory", "wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field", and "wherein the spare field is a reserved field or an open field in the instructions of said predetermined length instruction set" as recited in claim 1.

Therefore, Talcott does not teach or suggest the features of the present invention, as recited in claims 1, 8 and 9. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §102(b) rejection of claims 1, 8 and 9 as being anticipated by Talcott are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claims 1, 8 and 9.

Claims 1 and 12 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,948,053 to Augsburg, et al. ("Augsburg"). As indicated above, claim 12 was canceled. Therefore, this rejection with regard to claim 12 is rendered moot. This rejection with regard to the remaining claim 1 is traversed for the following reasons. Applicants submit that the features of the present invention, as now more clearly recited in claim 1, are not taught or suggested by Augsburg, whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, amendments were made to the claims to more clearly describe that the present invention is directed to a data processing device as recited, for example, in independent claim 1.

As previously discussed, the present invention, as recited in claim 1, provides a data processing device that decodes and executes instructions of a predetermined length instruction set, which contain a spare field. The data processing device

includes an instruction cache memory, a predecode-processor, and an instruction flow unit. The predecode-processor decodes operation codes contained in first fields of each of the instructions, so as to generate a piece of information. The information represents whether the instruction is a branch instruction or not. The predecode-processor also transfers the information as the spare field of each of the instructions. According to the present invention, the instruction cache memory holds the information in the spare field of each of the instructions. The instruction flow unit controls an executing sequence of the instructions based on information of the spare field, when executing instructions loaded from the cache memory. Also in the data processing device, the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that the instruction is a branch instruction, based on the information of the spare field. Furthermore, according to the present invention, the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set. The prior art does not disclose all these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record, particularly Augsburg, whether taken individually or in combination with any of the other references of record.

Augsburg discloses a method and system for calculating a branch target address. However, there is no teaching or suggestion in Augsburg of the data processing device of the present invention, as recited in the claims.

In Augsburg's method and system for calculating a branch target address, a branch instruction is fetched from memory. Upon fetching the branch instruction the

n-1 lower order bits of the branch target address may be pre-calculated and stored in the branch instruction prior to storing the branch instruction in the instruction cache. Upon retrieving the branch instruction from the instruction cache, the upper order bits of the branch target address may be recovered using the sign bit and the carry bit stored in the branch instructing. The sign bit and the carry bit may be used to select one of three possible upper-order bit combinations of the branch target address. The selected upper-order bit value combination may then be appended to the n-1 lower order bits of the branch target address to form the complete branch target address.

Features of the present invention, as recited in claim 1 include where the predecode-processor decodes operation codes contained in first fields of each of the instructions, so as to generate a piece of information. The information represents whether the instruction is a branch instruction or not. The predecode-processor also sets the information in the spare field of each of the instructions. According to the present invention, the instruction cache memory holds the information in the spare field of each of the instructions. Augsburg does not disclose this feature. For example, Augsburg does not teach or suggest where the instruction cache memory holds the information in the spare field of each of the instructions, in the manner claimed. In the present invention, the instruction cache memory holds the information in the spare field, where the information represents whether or not the instruction is a branch instruction or not, and where the spare field is a reserved field or an open field in the instructions of predetermined length instruction. This structure does not need to increase the capacity of the instruction cache because of the use of the spare field to temporarily store information of various types in that field. To the

contrary, Augsburg needs an extra memory device or memory area (see, e.g., the field 601 and column 3, lines 18-21). Therefore, Augsburg does not disclose the use of a spare field in the instructions of predetermined length instruction set, as in the present invention.

Other features of the present invention, as recited in claim 1, include where the instruction flow unit controls an executing sequence of the instructions based on information of the spare field, when executing instructions loaded from the cache memory. Also in the data processing device, the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that the instruction is a branch instruction, based on the information of the spare field. Furthermore, according to the present invention, the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set. Augsburg does not disclose these features. For example, Augsburg does not teach or suggest where the spare field is a reserved field or an open field in the instructions of the predetermined length instruction set, as in the present invention. As previously discussed, the instruction cache memory of the present invention holds the information in the spare field, where the information represents whether or not the instruction is a branch instruction or not, and where the spare field is a reserved field or an open field in the instructions of predetermined length instruction. This structure does not need to increase the capacity of the instruction cache because of the use of the spare field to temporarily store information of various types in that field. To the contrary, Augsburg needs an extra memory device or memory area (see, e.g., the field 601 and column 3, lines 18-21). Therefore, Augsburg does not

disclose the use of a spare field in the instructions of predetermined length instruction set, as in the present invention.

Therefore, Augsburg fails to teach or suggest "a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and sets the information in said spare field of each of said instructions" and "wherein the instruction cache memory holds the information in said spare field of each of said instructions" as recited in claim 1.

Furthermore, Aubsburg fails to teach or suggest "an instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory", "wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field", and "wherein the spare field is a reserved field or an open field in the instructions of said predetermined length instruction set" as recited in claim 1.

Therefore, Augsburg fails to teach or suggest the features of the present invention, as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §102(e) rejection of claim 1 are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference used in the rejection of claim 1.

35 U.S.C. §103 Rejections

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Talcott. As indicated above, claim 12 was canceled. Therefore, this rejection is rendered moot.

Claims 8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Augsburg in view of Nishimukai, further in view of U.S. Patent No. 6,499,712 to Irie, et al. ("Irie"). This rejection is traversed for the following reasons. Applicants submit that claims 8 and 9 are dependent on claim 1. Therefore, claims 8 and 9 are allowable for at least the same reasons previously discussed regarding independent claim 1. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

In view of the foregoing amendments and remarks, Applicants submit that claims 1, 8 and 9 are in condition for allowance. Accordingly, early allowance of claims 1, 8 and 9 is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. H-1098).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

Donna K. Mason
Registration No. 45,962

DKM/cmd
(703) 684-1120